

and the like can be also used.

The same unit of one display pixel is used for both of the moving image and the still image in the embodiment. However, since the precision as high as that of the still image is not generally required in the moving image, (2×2) or arbitrary $(h \times i)$ display pixels in the still image can be used as a unit of display pixels in the moving image. When signals are written to the $(h \times i)$ display pixels at the same timing, unnecessary increase in writing speed can be prevented.

An image signal accuracy of about 6 bits is requested in the moving image and that of about 8 bits is required in the still image. Consequently, when the accuracy of the A/D converter of the moving image signal output circuit 43 and that of the still image signal output circuit 41 are changed to 6 bits and 8 bits, respectively, the bit accuracy of the moving image signal output circuit 43 which is requested to operate at higher speed becomes lower, so that designing of the A/D converter is facilitated.

Although a case where one moving picture display area is surrounded by one still picture display area has been described in the embodiment, according to the idea of the invention, if the moving and still picture

display areas having different frame rates exist, the effects of the invention can be obtained irrespective of the number of areas and arrangement of the areas. The effects of the invention can be also obtained when
5 still picture display areas having different frame rates are neighboring.

Second embodiment

A second embodiment of the invention will be described hereinbelow with reference to Fig. 5. Fig. 5
10 is a diagram illustrating the construction of a child device 60 in the embodiment. Since the construction and operation of the parent device 31 are similar to those in the first embodiment, their description are omitted here.

15 The difference between the present embodiment and the first embodiment is as follows. In the first embodiment, the elements from the radio interface 2 to the signal generating circuit 17 are constructed by an electronic circuit as hardware. On the contrary, in
20 the second embodiment, the same function is realized by software on a microcomputer 61 and an image memory 62 having parallel output ports. The second embodiment can also obtain effects similar to those of the first embodiment.

25 Especially, when the number of output ports of the

image memory 62 is set to the same as the number of pixels in the column direction of the display pixel array part, it is convenient from the viewpoint of the layout of the signal generating circuit 17.

5 Third embodiment

A third embodiment of the invention will be described hereinbelow with reference to Fig. 6. Fig. 6 is a diagram showing the construction of a write signal generating circuit 71 and a display pixel array 10 72 according to the third embodiment. The difference of the third embodiment from the first embodiment is that a two-gradation still image signal output circuit 63 is provided and an output of the two-gradation still image signal output circuit 63 is used to write 15 binary image data.

In case of using the two-gradation still image signal output circuit 63, an A/D converter is unnecessary so that power consumption is very small. For image data using monochromatic color or only 20 multicolors of 8 colors, the power source of the still image signal output circuit 41 is temporarily stopped, thereby enabling the power consumption to be reduced.

Fourth embodiment

A fourth embodiment of the invention will be 25 described hereinbelow with reference to Fig. 7. Fig. 7